WHAT IS CLAIMED IS:

1. A communication device for performing communication using a first and second clock signals complementary to each other, comprising:

a squelch detection circuit for determining the communication device as being in a data communication state to output a first signal when said received first and second clock signals have a potential amplitude larger than a predetermined value, and for determining the communication device as being in a non data communication state to output a second signal when said first and second clock signals have a potential amplitude not more than said predetermined value; and

an initialization circuit for initializing said communication device when the second signal is outputted from said squelch detection circuit.

2. The communication device according to claim 1, further comprising:

a receiver for regenerating a data signal on the basis of said received first and second clock signals, wherein

said receiver includes:

first and second capacitors having electrodes receiving said first and second clock signals, respectively; and

a differential amplification circuit including first and second transistors having gates connected to another electrodes of said first and second capacitors and having first electrodes connected to each other, respectively, and amplifying the potential difference in the gates of said first and second transistors, and

said initialization circuit sets the potentials of the gates of said first and second transistors to predetermined potentials when the second signal is outputted from said squelch detection circuit.

3. The communication device according to claim 1, further comprising:

a receiver for regenerating a data signal on the basis of said received

first and second clock signals; and

an internal clock generation circuit for outputting an internal clock signal in synchronization with said data signal generated by said receiver, wherein

said internal clock generation circuit includes:

a frequency comparison circuit for comparing the frequency of said data signal with the frequency of said internal clock signal, and outputting a frequency difference signal according to comparison results;

a phase comparison circuit for comparing the phase of said data signal with the phase of said internal clock signal, and outputting a phase difference signal according to comparison results;

a charge pump for selectively outputting a positive current or negative current in response to said frequency difference signal and said phase difference signal;

a loop filter including a capacitor for accumulating the output current of said charge pump to output a control voltage; and

a voltage control oscillator for outputting a clock signal having a frequency according to said control voltage, as said internal clock signal, and

said initialization circuit sets said control voltage to a predetermined value when the second signal is outputted from said squelch detection circuit.

4. The communication device according to claim 3, wherein

said initialization circuit includes:

first and second resistance elements each having a predetermined resistance value; and

a switching circuit for connecting said first resistance element between the line of a power supply potential and an output node of said loop filter, and also connecting said second resistance element between the line of a reference potential and the output node of said loop filter when the second signal is outputted from said squelch detection circuit.

5. The communication device according to claim 3, wherein said initialization circuit includes:

a switching circuit for applying said data signal to said frequency comparison circuit and said phase comparison circuit when the first signal is outputted from said squelch detection circuit, and applying a reference clock signal having a predetermined frequency to said frequency comparison circuit and said phase comparison circuit when the second signal is outputted from said squelch detection circuit.

6. The communication device according to claim 3, wherein said initialization circuit includes:

a switching circuit for applying said data signal to said frequency comparison circuit when the first signal is outputted from said squelch detection circuit, and applying a reference clock signal having a predetermined frequency to said frequency comparison circuit when the second signal is outputted from said squelch detection circuit.